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TRANSMITTAL FORM

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Total Number of Pages in This Submission: 26

Application Number	10/681,507
Filing Date	October 7, 2003
First Named Inventor	Michael A Vyvoda
Art Unit	2813
Examiner Name	Laura M. Schillinger
Attorney Docket Number	MA-075-I

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
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- ☑ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Matrix Semiconductor, Inc.		
Signature			
Printed name	Pamela J. Squyres		
Date	December 12, 2005	Reg. No.	52,246

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Signature			
Typed or printed name	Pamela J. Squyres	Date	12/12/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 3558P027D

In re patent application of
Michael A. Vyvoda et al.

Serial No. 10/681,507 Group Art Unit: 2813

Filed: October 7, 2003 Examiner: Laura M. Schillinger

For: ELECTRICALLY ISOLATED PILLARS IN ACTIVE DEVICES

BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 12, 2005

To the Commissioner:

Appellants hereby appeal the June 14, 2005 final rejection of claims 1-6 and 8-12 in the above-identified application to the Board of Patent Appeals and Interferences.

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Pamela J. Squyres, reg. no. 52,246

Dec. 12 2005
Date of Deposit

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Matrix Semiconductor, Inc., a Delaware corporation.

II. RELATED APPEALS AND INTERFERENCES

An appeal was filed in related US Patent Application No. 10/681,504 on July 18, 2005. US Patent No. 6,952,043, hereinafter the '043 patent, is the parent of both related US Patent Application No. 10/681,504, which is a continuation of the '043 patent, and the present application is, which is a divisional application of the '043 patent.

III. STATUS OF CLAIMS

Claims 1-67 are pending in the application. Claims 13-67 are withdrawn from consideration. Claims 1-6 and 8-12 have been finally rejected and are the subject of this appeal. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. A listing of the appealed claims is presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

No amendments after final rejection were filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A monolithic three dimensional memory array is formed using a method to avoid formation of defects called *stringers*.

In conventional memories, memory cells are formed on a single level in the surface of a substrate, typically a monocrystalline silicon wafer. In contrast, a monolithic three dimensional memory array includes multiple memory levels formed *above* the substrate, stacked one atop another. Vertical stacking allows the memory to be highly dense.

In one form of monolithic three dimensional memory array, each memory level includes parallel bottom conductors, extending horizontally, and parallel top conductors, also extending horizontally, the top conductors above the bottom conductors. The top and bottom conductors are perpendicular to one another and parallel to the wafer surface, forming a cross-point array. Between each bottom conductor and each top conductor, at their intersection, is a pillar. Each memory cell includes a portion of a bottom conductor, a pillar, and a portion of a top conductor. The bottom conductor, pillar, and top conductor include doped silicon layers and a dielectric antifuse layer, arranged to form a P-N diode and an antifuse. The memory cell is a one-time programmable memory cell programmed by rupturing the antifuse.

A monolithic three dimensional memory array having such a structure and function is taught in Johnson et al., US Patent No. 6,034,882, owned by the assignee of the present invention.

The array of Johnson et al. was formed using a high degree of self-alignment. Briefly, 1) the layers of the bottom conductors and the pillars were blanket deposited, the pillar layers above the bottom conductor layers. The pillar layers were silicon layers. 2) A first pattern-and-etch step was performed to etch the deposited layers, forming first parallel rails, the first rails including the layers of the pillars and the layers of the bottom conductors. 3) After dielectric fill and planarization to expose the tops of the first rails, the layers of the top conductors were deposited above the fill and first rails. Dielectric fill is used to provide electrical isolation and structural support between patterned features. 4) A second pattern-and-etch step also formed parallel rails, these rails perpendicular to the first rails. This pattern-and-etch step etched the layers of the top conductors, then continued, etching the layers of the pillars. The second etch stopped before etching the bottom conductors.

As is well known, most etchants are selective, etching some materials but not others. Both pattern-and-etch steps etched only the active layers, the top conductor layers, the pillar layers, and the bottom conductor layers, but did not etch the intervening dielectric fill.

The layers of the bottom conductors were etched in only the first pattern-and-etch step, and thus were in the form of rails. The layers of the top conductors were etched in only the second pattern-and-etch step, and thus were also in the form of rails. The layers of the pillars, between the top conductor and bottom conductor layers, were etched in *both* pattern-and-etch steps, which were perpendicular to each other, and thus were in the form of pillars, each pillar having a square cross-section. Considering the cross-section of each pillar, two opposing edges of each pillar were aligned with the edges of the bottom conductor below it, while the other two opposing edges of the pillar were aligned with the edges of the top conductor above it.

This fabrication method minimized the number of masking steps, which are very expensive, and was thus advantageous. It suffered a disadvantage, however, which made the resulting memory prone to defects.

The etch during the two pattern-and-etch steps described was intended to be perfectly anisotropic, producing perfectly vertical sidewalls on the conductors and pillars. In reality, however, no etch is perfectly anisotropic, and some lateral etching of sidewalls occurs. The result is that rather than being perfectly vertical, etched sidewalls tend to be sloped so that an etched trench (the gap between rails, say) tends to be slightly wider at the top than at the bottom.

Thus the first pattern-and-etch step of Johnson et al. tended to produce parallel first rails which were slightly wider at the bottom than at the top. Next the gaps between the first rails were filled with dielectric material. The shape of each strip of dielectric material was the inverse of that of the rails, and necessarily wider at the top than at the bottom. Dielectric material, then, was slightly overhanging the material of the adjacent first rail.

After deposition of the top conductor layers, the second pattern-and-etch step was performed. This etch formed the top conductors, then continued to etch the pillar layers. Recall that the pillar layers are silicon, and that during the pillar etch, silicon is etched, while the dielectric fill is not. Thus between the pillars, overhanging dielectric material shielded a small volume of silicon from the etchant during the second pattern-and-etch step, preventing it from being removed as intended. These small remainders of silicon, called stringers, could

connect a pillar to an adjacent pillar, forming a conductive path between structures that were intended to be electrically isolated, and creating a short.

Turning now to the present invention, the sequence of events is changed, creating a structure similar to that of Johnson et al., while avoiding this harmful stringer formation.

Fabrication in the present invention begins as in Johnson et al.: 1) The layers of the bottom conductors and of the pillars are deposited. 2) A first pattern-and-etch step is performed, forming parallel first rails.

At this point, however, is an important difference: 3) *Before* the dielectric fill is deposited between the first rails, in the present invention a second pattern-and-etch step is performed, perpendicular to the first, forming the pillars. These first and second patterning steps are formed back-to-back, with no dielectric fill deposition step between them. Since no dielectric fill is deposited between these back-to-back patterning steps, no dielectric material intervenes between the pillars to shield any stringer material from etchant; thus no stringers are formed. It is novel to perform two patterning steps back-to-back with no dielectric fill step between them.

Fabrication continues: After dielectric fill and a planarization step to expose tops of the pillars, 4) the top conductor layers are deposited, and 5) a third pattern-and-etch step forms the top conductors.

Compared to Johnson et al., the method of the present invention requires an additional masking step, but stringer formation, to which Johnson et al. was susceptible, is avoided.

The present invention, then, is a method to form an active device by performing two patterning steps back-to-back, with no intervening dielectric fill step between them, in which at least some layers are patterned and etched in both patterning steps.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

There is a single ground of rejection to be reviewed in this appeal: Whether claim 1 and its dependent claims 2-6 and 8-12 102(a) are anticipated by Lee et al., US Patent Application No. 09/927648 and what the Examiner refers to as Admitted Prior Art (APA).

VII. ARGUMENT

A. Claims 1 is Not Anticipated by Lee et al.

Claim 1 recites a method of forming an active device, the method comprising: performing a first patterning operation on a first plurality of layers, the first patterning operation defining a first feature of the active device; and performing a second patterning operation on at least one patterned layer of the first plurality of layers, the second patterning operation defining a second feature of the active device, wherein the first and second patterning operations are performed substantially back-to-back.

Appellants point out that the claim recites that the two patterning steps "are performed substantially back-to-back." As described in the specification of the present invention, the term "back-to-back" specifically means that the second patterning operation is performed immediately after the first, *without the interposition of a dielectric fill step.* A purpose of the present invention is to prevent the unintended formation of conductive "stringers" which provide unwanted electrical connections between adjacent pillars. The stringers are formed when conductive material is trapped underneath overhanging dielectric fill during the second etch. In the present invention, by forming the pillars in two back-to-back patterning steps, with no dielectric fill deposited between the patterning steps, no stringers can be formed.

The Examiner points to col. 19, lines 29-47 and Figs. 9a and 9b of Lee et al.:

> Alternatively, as shown in FIGS. 9A and 9B, a pillar can be formed by the intersection of the patterning of the first and second I/O's. For example, a pillar can be formed by first blanket depositing a first I/O conductor 900 followed by the sequential blanket deposition of the film stack 902 (e.g., N+/P-/N+) of the desired pillar. The first I/O film 900 and the pillar film stack 902 are then etched to form a plurality of pillar strips 904 as shown in FIG. 9a. During subsequent processing to pattern the second I/O, the second I/O 906 is etched in a direction perpendicular or orthogonal to the plurality of strips 904. The etch step used to pattern the second I/O 906 is continued so as to etch away the pillar film stack 902 from the portions of the strip 904 which are not covered or masked by the second I/O 906. In this way, a pillar 908 is formed at the intersection of the first and second I/O's. The pillar 908 is formed in direct alignment with the intersection or overlap of the first and

> second I/O's. The intersection technique of forming a pillar is advantageous because it saves additional lithography steps.

In the procedure described in this paragraph, the first patterning step forms pillar strips 904, shown in Fig. 9a, which include semiconductor stack 902 and first conductor 900. A second patterning step, orthogonal to the first, forms the top conductor ("second I/O") 906 and continues through semiconductor stack 902, forming pillars 908 shown in Fig. 9b. The Examiner considers these two patterning steps to be back-to-back.

It would be clear to one skilled in the art of photolithography and etch, however, that these steps *cannot* be back-to-back.

Declaration under 37 CFR 1.132: Etches of Fig. 9a and 9b not back-to-back

A declaration under 37 CFR 1.132 by James M. Cleeves, an inventor of Lee et al., was submitted with a response after the final rejection attesting that the two etch steps are not performed back-to-back, and that a dielectric fill step (along with a planarization step and another deposition step) are performed between them, and thus that these steps are not performed back-to-back. This declaration is included in the Evidence Appendix.

Etch steps cannot be back-to-back

As described in the specification of the instant application, and as is well known in the art, it is conventional, after a pattern-and-etch step, to deposit dielectric fill to fill the gaps between the just-patterned features, providing structural support to those patterned features and for layers to be deposited in later steps.

Fig. 9a of Lee et al. shows the structure after a first patterning step, when strip 904 has been formed. Fig. 9a of Lee et al. is a perspective view. For convenience, Figs. 9a and 9b of Lee et al. are included in Exhibit B of the Evidence Appendix. In Exhibit C, also included in the Evidence Appendix, Fig. 1 shows the same structure in a cross-sectional view. In the view of Fig. 1, the long dimension of strip 904 extends out of the page.

Fig. 9b of Lee et al. shows the structure after (as Appellants will show) a dielectric fill step, a step to deposit conductor material which will form top conductor 906, and a pattern and etch step forming top conductor 906 and etching pillar 908.

Fig. 2 of Exhibit B shows the structure of Fig. 9b (a perspective view) in cross-section, in the same view as Fig. 1. Fig. 9b of Lee et al. shows the top conductor 906 extending, apparently unsupported, into space atop pillar 908, perpendicular to bottom conductor 900. In reality top conductor 906 is supported by dielectric fill, as shown in Fig. 2. If no dielectric fill step had been performed after the patterning step to form strip 904, top conductor 906 would have nothing to support it, and would have the form shown in Fig. 3 of Exhibit B. As noted, it is conventional to perform a dielectric fill step following a patterning step to provide such support. It is also conventional to omit dielectric fill in perspective views, as it would obscure the active devices, which are generally of interest.

Appellants concede that no dielectric fill step is *explicitly* listed in the description of col. 19, lines 29-47 of Lee et al.; this step is so conventional as to have been omitted from the description, along with other conventional cleaning steps that were likely performed. But the only reasonable explanation for the shape of top conductor 906 is the presence of dielectric fill, supporting it from beneath, and one skilled in the art would assume its presence. A dielectric fill step was necessarily performed between the two patterning steps of Lee et al. described in col. 19, lines 29-47, and thus these two patterning steps are not back-to-back.

Appellants have shown that claim 1 and its dependent claims 2-13 distinguish over the cited art.

CONCLUSION

Accordingly, Appellants respectfully solicit the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

Dec. 12, 2005
Date

Pamela J. Squyres Reg. No. 52,246

Matrix Semiconductor, Inc.
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(408) 869-8923 (fax)

This Appeal Brief is being filed together with authorization to charge $500 (large entity) covering the appeal fee to the undersigned deposit account 502302. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 502302.

Dec. 12, 2005
Date

Pamela J. Squyres Reg. No. 52,246

VIII. CLAIMS APPENDIX

1. A method of forming an active device, the method comprising:

performing a first patterning operation on a first plurality of layers, the first patterning operation defining a first feature of the active device; and

performing a second patterning operation on at least one patterned layer of the first plurality of layers, the second patterning operation defining a second feature of the active device, wherein the first and second patterning operations are performed substantially back-to-back.

2. The method of Claim 1, wherein the first patterning operation includes:

etching the first plurality of layers into a first plurality of strips oriented in a first direction.

3. The method of Claim 2, wherein the second patterning operation includes:

etching at least one strip of the first plurality of strips in a second direction, the second direction being different than the first direction, to create a pillar.

4. The method of Claim 3, wherein at least one strip of the first plurality of strips comprises a first terminal of the active device.

5. The method of Claim 4, wherein the pillar comprises another portion of the active device.

6. The method of Claim 4, further including:

depositing a first dielectric after both first and second patterning operations; and

planarizing the first dielectric to expose a surface of the active device.

7. (Allowed)

8. The method of Claim 6, further including:

depositing a second plurality of layers on the surface of the active device and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

9. The method of Claim 8, wherein said second plurality of strips is not self-aligned to the pillar.

10. The method of Claim 8, wherein at least one strip of the second plurality of strips comprises a second terminal of the active device.

11. The method of Claim 1, wherein the first plurality of layers includes an antifuse layer fully etched through by the first patterning operation, but not fully etched through by the second patterning operation.

12. The method of Claim 1, wherein the first plurality of layers includes an antifuse layer fully etched through by both the first and second patterning operations.

13.-67. (Withdrawn)

IX. EVIDENCE APPENDIX

Exhibits A, B, and C, following this sheet, are included as evidence.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Vyvoda et al.	
Application No.: 10/681,507	Group Art Unit: 2813
Filed: 10/07/2003	
Title: Electrically Isolated Pillars in Active Devices	Examiner: Laura M. Schillinger
Attorney Docket No.: 3558P027D	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 18, 2005

DECLARATION UNDER 37 CFR §1.132

To the Commissioner:

As an inventor of Lee et al., US Patent No. 6,881,994 and one skilled in the art of submicron semiconductor fabrication, I, James M. Cleeves, hereby declare my opinion that:

1. Formation of the structure pictured in Figs. 9a and 9b of Lee et al., US Patent No. 6,881,994, involves two patterning steps. The first patterning step forms strip 904. The second patterning step forms conductor 906 and pillar 908. Though not shown, dielectric fill is supporting the apparently unsupported section of conductor 906. This dielectric fill was deposited in a dielectric fill step performed between the first and second patterning steps. Other steps are also performed after the deposition of dielectric fill and before the second patterning step, including polish of dielectric fill to expose the top of strips 904

and deposition of layer 906. The first and second patterning steps forming the structure of Figs. 9a and 9b of Lee et al. thus are not performed back-to-back, i.e. with no intervening dielectric fill step.

2. From Figs. 9a and 9b of Lee et al. and the accompanying description, one skilled in the art of submicron semiconductor fabrication would assume that a dielectric fill step, as well as a polishing step to expose the tops of strips 904 and a deposition step to deposit layer 906, was performed between the two patterning steps that form the structure of Figs. 9a and 9b, and thus that these patterning steps are not performed back-to-back with no intervening dielectric fill step, even though this dielectric fill step is not explicitly detailed in the description of Figs. 9a and 9b.
3. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful statements may jeopardize the validity of the application or any patent issuing therefrom.

Respectfully submitted,

James M. Cleeves

8/18/05
Date

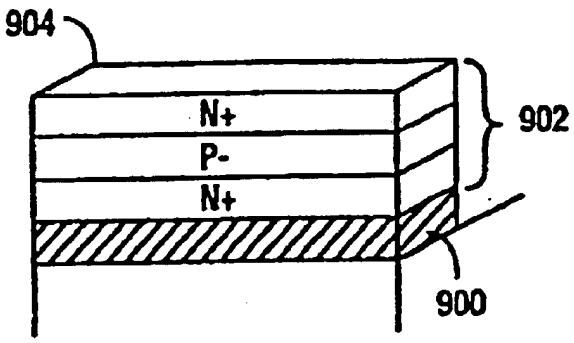

FIG. 9A

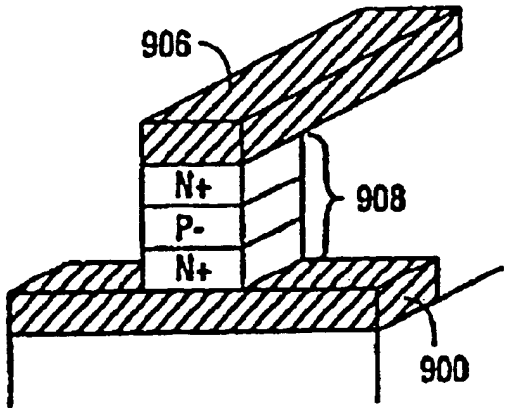

FIG. 9B

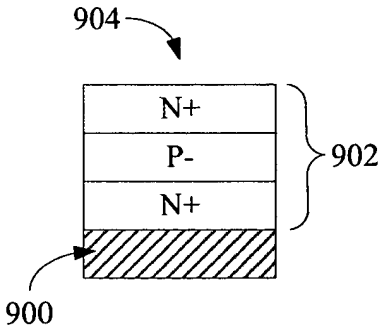

Fig. 1

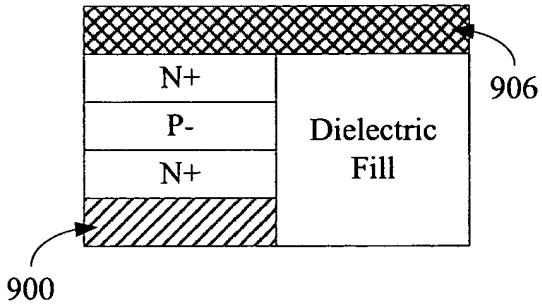

Fig. 2

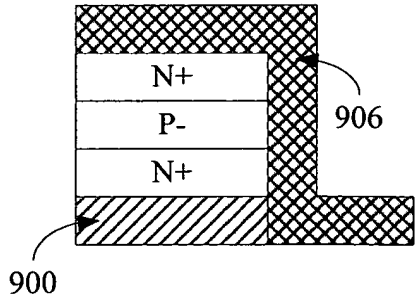

Fig. 3

X. RELATED PROCEEDINGS APPENDIX

At the time of filing this appeal brief, no decision has been rendered in the related appeal of US Patent Application No. 10/681,504.